REMARKS/ARGUMENTS

In response to the Examiner's final Office Action of September 5, 2007 issued with respect to the present RCE application, the Applicant submits the accompanying Request for Continued Examination and Amendment of the claims, and the below Remarks.

Regarding Amendment

In the Amendment:

independent claim 1 is amended to clarify that the clock filter has a temperature sensor which is configured to detect an under temperature condition of the integrated circuit and to prevent output of the system clock to logic circuitry of the integrated circuit upon detection of the under temperature condition. Support for this amendment can be found in dependent claim 3 and at paragraphs [8088]-[8090] of the originally filed specification;

dependent claim 3 is cancelled accordingly;

dependent claim 4 is amended to depend directly from amended independent claim 1; and

pending dependent claims 5 and 6 are unchanged.

It is respectfully submitted that the above amendments do not add new matter to the present application.

Regarding 35 USC 112, second paragraph Rejections

It is respectfully submitted that the above-described amendments of independent claim 1 to clarify that a temperature sensor of the clock filter detects the under temperature condition and prevents output of the system clock clarifies the recitation of claims 1 and 4-6.

35 USC 102(e) and 103(a) Rejections

It is respectfully submitted that the subject matter of amended independent claim 1, and claims 4-6 dependent therefrom, is not disclosed or suggested by either of newly cited Uchida et al. (US 6,731,919) and Yamazaki (JP 09-212254) either taken alone or in combination with either of previously cited Chemla and Kitano, for at least the following reasons.

As discussed above, independent claim 1 has been amended to clarify that when an under temperature condition of the integrated circuit is detected output of the system clock to logic circuitry of the integrated circuit is prevented. In this way, damage to the integrated circuit caused by an attacker attempt to introduce race-conditions of the logic circuitry by increasing the clock signal frequency due to decreased temperatures can be prevented (see paragraphs [8088]-[8090] of the originally filed specification).

On the other hand, both Uchida and Yamazaki (like previously cited Kawai) specifically disclose increasing clock signal frequency when decreased operating temperatures are detected (see col. 4, line 50-col. 6, line 14 of Uchida, and abstract and paragraph [0039] of Yamazaki), which is contrary to the operation recited in the claimed invention.

Further, both Chemla and Kitano only disclose stopping a clock signal within an integrated circuit when an over temperature conditions is detected (see col. 3, line 48-col. 4, line 44 of Chemla, and col. 5, line 8-52 of Kitano).

Thus, in any combination of Chemla and Kitano with Yamazaki (or Uchida), one of ordinary skill in the art would be motivated to increase the clock frequency upon detection of under temperature conditions, and to only stop the clock signal upon detection of over temperature conditions, which is clearly different that the recitation of amended independent claim 1, and claims 4-6 dependent therefrom.

It is respectfully submitted that all of the Examiner's rejections have been traversed. Accordingly, it is submitted that the present application is in condition for allowance and reconsideration of the present application is respectfully requested.

Very respectfully,

Applicant:

SIMON ROBERT WALMSLEY

C/o: Silverbrook Research Pty Ltd
393 Darling Street
Balmain NSW 2041, Australia

Email: kia.silverbrook@silverbrookresearch.com

Telephone: +612 9818 6633

Facsimile: +61 2 9555 7762